

## WHAT IS CLAIMED IS:

1. A dynamic associative memory device, comprising:
  - a word line;
  - 5 a pair of first bit line (BL) and second bit line (/BL) which has signal potentials opposite to the first bit line;
  - a plurality of memory cells, wherein each of the memory cells includes;
    - 10 a data-storing capacitor connected to the first bit line or the second bit line through first transmission gate capable of being switched to ON-state in accordance with an activation of the word line, and having a cell plate supplied with a source voltage; and
    - 15 at least one second transmission gate provided in series between the first bit lines and the second bit line, capable of being switched to ON-state in response to a memory node potential at an opposite side of a source voltage supply-side of the data-storing capacitor;
  - 20 and
    - a memory cell initializing circuit for controlling the memory node potential upon receiving a reset signal so that at least one of the second transmission gates is switched to OFF-state.

2. The dynamic associative memory device according to  
Claim 1,

wherein said memory cell initializing circuit  
activates the word line and controls the memory node  
5 potential upon receiving the reset signal so that at least  
one of the second transmission gate is switched to OFF-  
state.

3. The dynamic associative memory device according to  
10 Claim 1,

wherein the memory-cell initializing circuit sets  
the memory-node potential to 0 volt upon receiving the  
reset signal.

15 4. A dynamic associative memory device, comprising:

a word line;

a pair of first bit line (BL) and second bit line  
(/BL) which has signal potentials opposite to the first bit  
line;

20 a sense-amplifier to amplify the difference of  
potentials between the first bit lines and the second bit  
line;

a plurality of memory cells, wherein each of the  
memory cells includes;

25 first and second data-storing capacitor

connected to the first bit line and the second bit line through each of two first transmission gates each capable of being switched to ON-state in accordance with an activation of a word line, and having a cell plate supplied  
5 with a source voltage; and

two second transmission gates provided in series between the first bit lines and the second bit line, of which each gate is connected to a memory node that is an opposite side node of a source voltage supply-side  
10 node of the first and second data-storing capacitor each capable of being switched to ON-state in response to the memory node potential; and

a memory cell initializing circuit for controlling the memory node potential by activating the  
15 word line and the sense-amplifier upon receiving a reset signal so that at least one of the second transmission gates is switched to OFF-state.

5. The dynamic associative memory device according to  
20 Claim 4,

wherein the memory-cell initializing circuit sets one of the memory-node potentials to 0 volt upon receiving the reset signal.